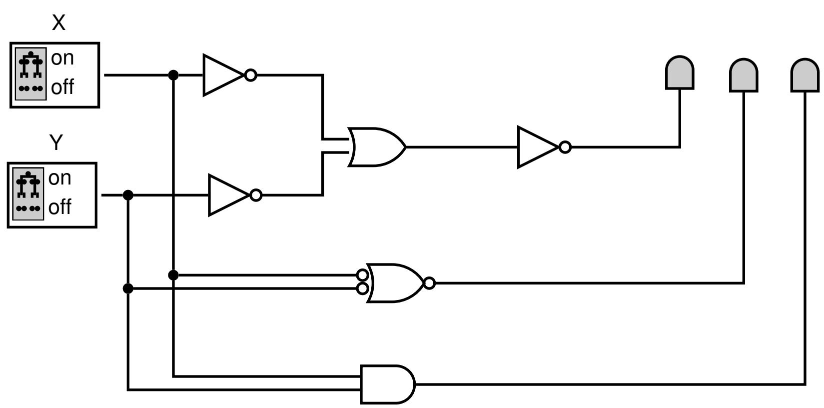
3. Suppose that you only have a collection of or and not gates. Design a circuit that implements the and function.

a	b	ab	not a	not b	not a + not b
0	0	0	1	1	1
0	1	0	1	0	1
1	0	0	0	1	1
1	1	0	0	0	0

You will notice that the last column in the table is nand, so not this.

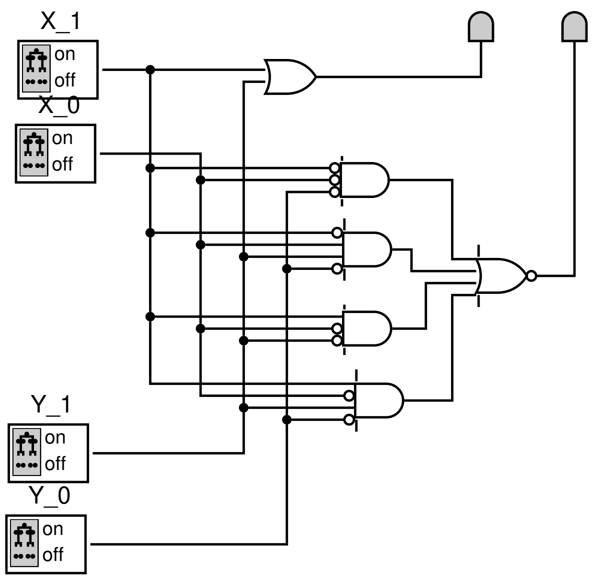


10 Design a circuit that takes two 2-bit inputs and produces a 2-bit output that is the larger of the inputs when they are interpreted as binary numbers.

x1	x0	y1	y0	z1	z0
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	1	0	1
0	1	1	0	1	0
0	1	1	1	1	1
1	0	0	0	1	0
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	1	1
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

Notice that z1 = x1+y1

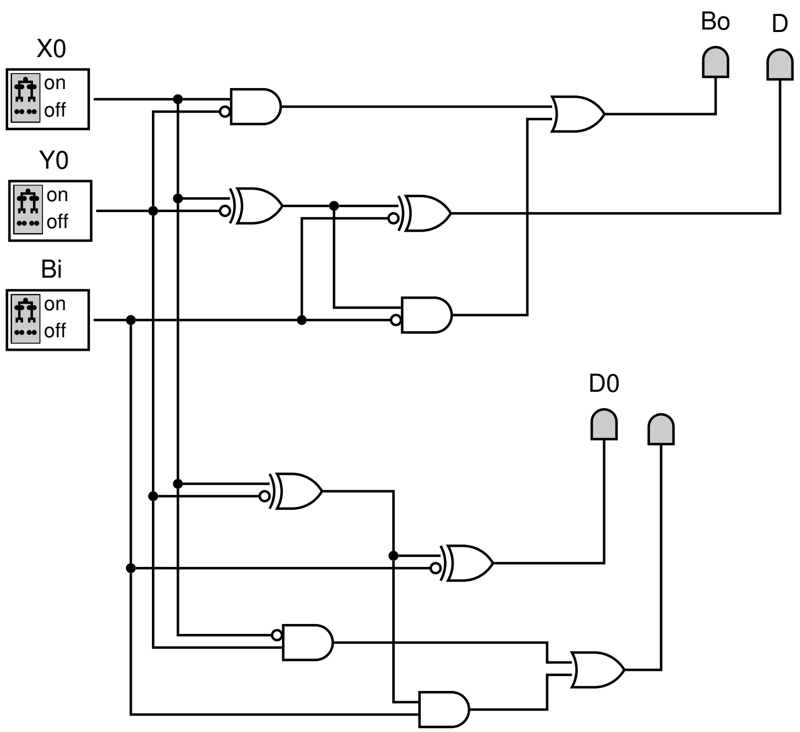
z0 us more complex but can be found with some boolean algebra



Designer:		**Document:**	hw3.v
Site:	Earth	**Page:**	2 of 5
Date:	March 5, 2003	**Module:**	Q_10

TKGate 1.6i

8a Consider the relationship between binary addition and subtraction. Using a table, prove that the following circuit implements a full subtractor for the expression x-y



Truth Table for this Circuit

Bi	X	Y	Bo	D
0	0	0	1	0
0	0	1	0	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	1	0
1	1	1	0	1

But for subtraction

Bi	X	Y	D	Bo
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

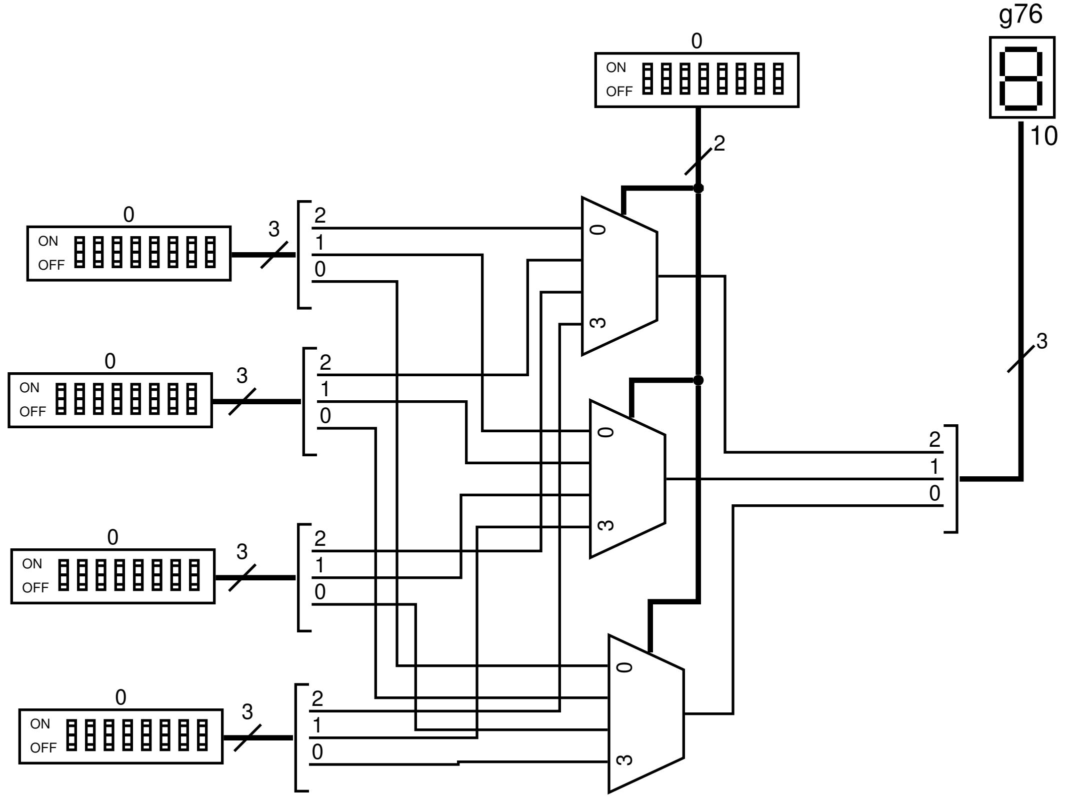
bi = 0	bi = 1
0-0 = 0, b=0	0-0-1 = 1, b=1
0-1 = 1, b=1	0-1-1 = 0, b=1
1-0 = 1, b=0	1-0-1 = 0, b=0
1-1 = 0, b=0	1-1-1 = 1, b=1

Notice the difference bit is right.

Designer:		**Document:**	hw3.v
Site:	Earth	**Page:**	3 of 5
Date:	March 5, 2003	**Module:**	Q_8

TKGate 1.6i

Given 3 4-> 1 multiplexers, show how you could construct a 12->3 multiplexer, that is, a 3x(4->1) multiplexer.



Designer:		**Document:**	hw3.v
Site:	Earth	**Page:**	4 of 5
Date:	March 5, 2003	**Module:**	Q22

TKGate 1.6i

Homework 3, Computer Architecture.

P 64,
- 3,
- 8a Implement your solution in TK-GATE
- 10 I would expect a truth table.
- 22
- Design a 4 bit register,
  - load,
  - shift right,
  - shift left,
  - fill bit